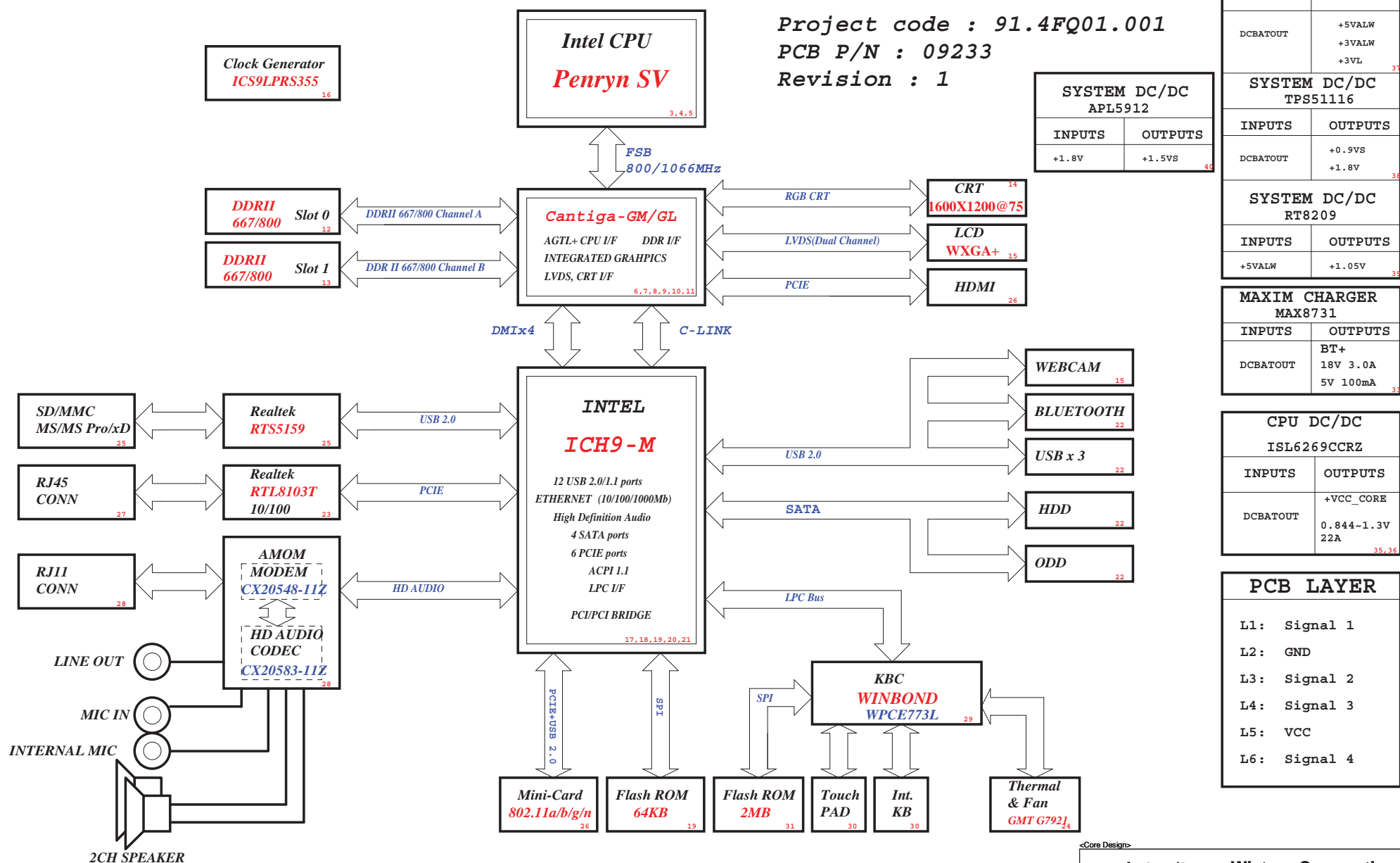


HBU16-1.2 Intel UMA Block Diagram

Project code : 91.4FQ01.001

PCB P/N : 09233

Revision : 1



<http://laptop-motherboard-schematic.blogspot.com/>

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Block Diagram

Size

Document Number

HBU16 1.2

Date _____

Monday, July 06, 2009

Sheet 1

Rev

1CH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI CS1#/GPIO58	Boot BIOS Destination Selection 0:1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

PCIE Routingpage 19

LANE1	LAN
LANE2	MiniCard WLAN

USB Tablepage 19

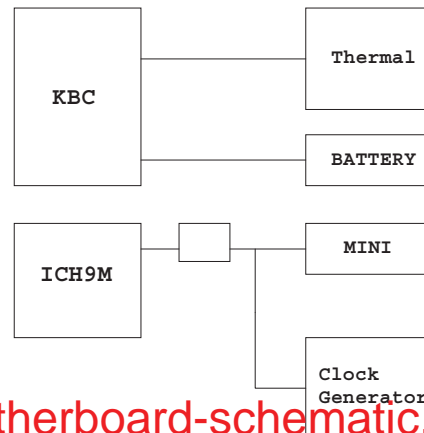
USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

SMBus



Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (Default)
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

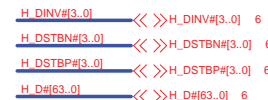
NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

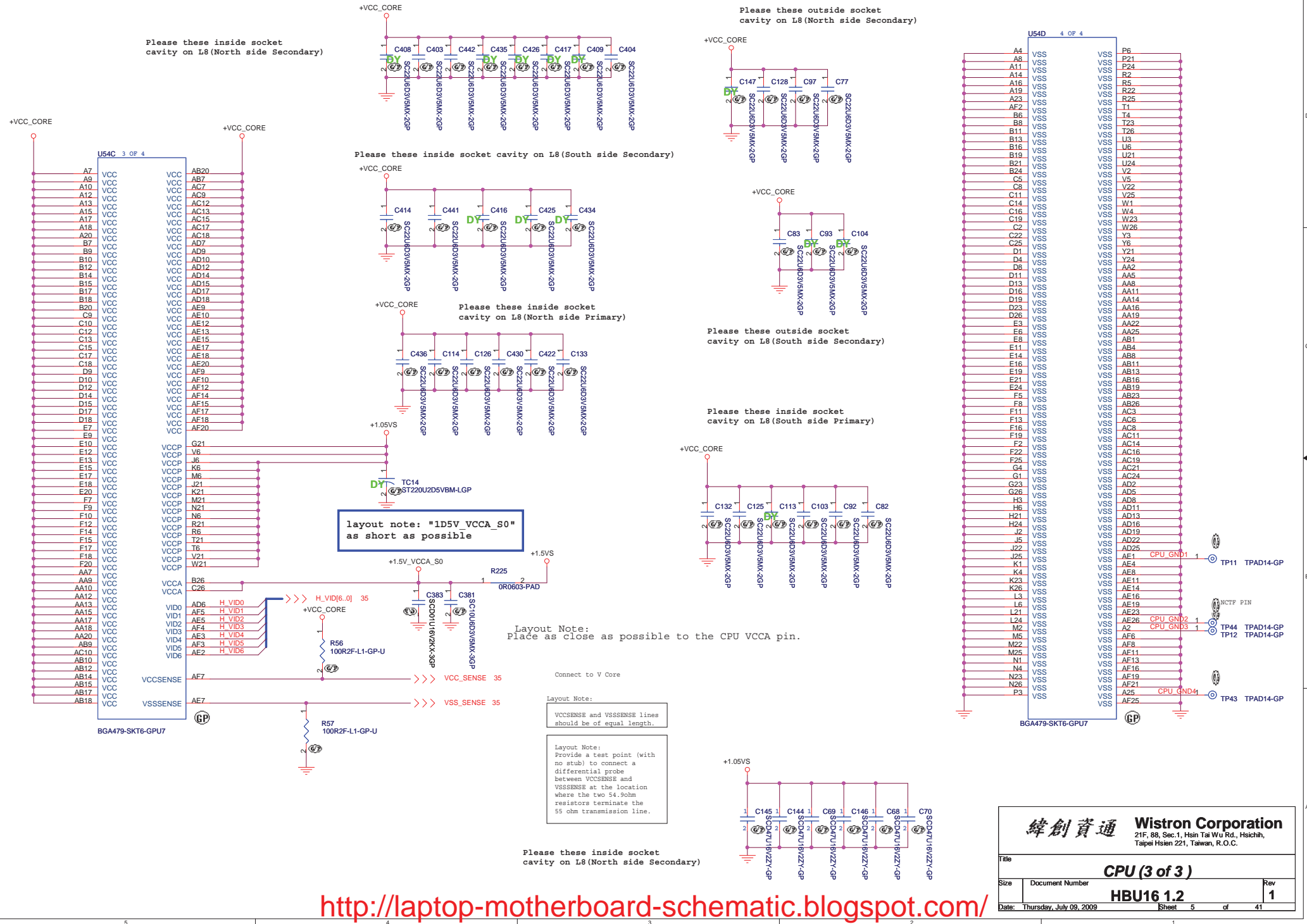
<http://laptop-motherboard-schematic.blogspot.com/>


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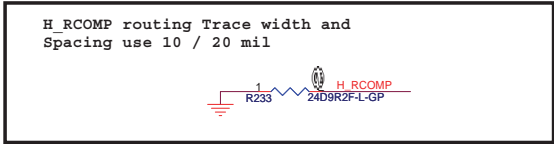
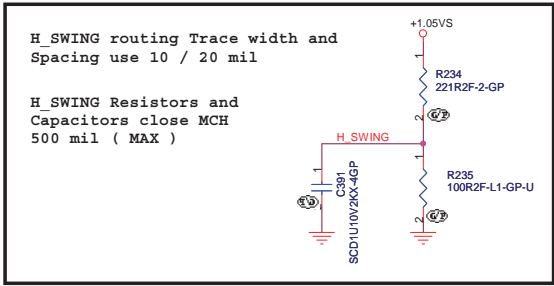
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Date:	Tuesday, June 30, 2009	Sheet 2	of 41



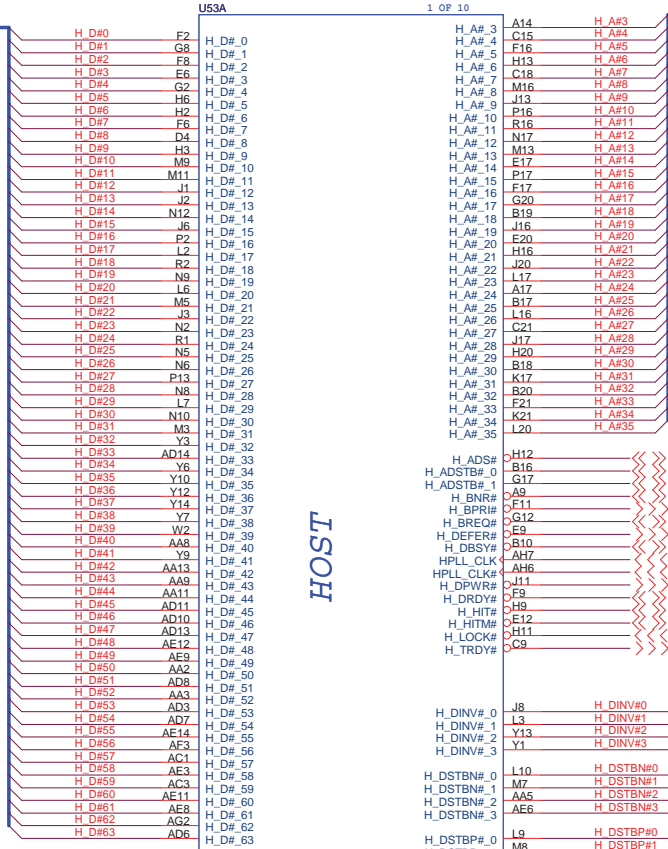
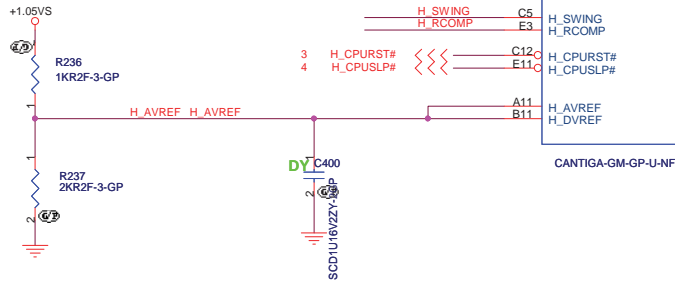
Layout Note:
Comp0, 2 connect with $Z_0=27.4$ ohm, make
trace length shorter than 0.5" .
Comp1, 3 connect with $Z_0=55$ ohm, make
trace length shorter than 0.5" .

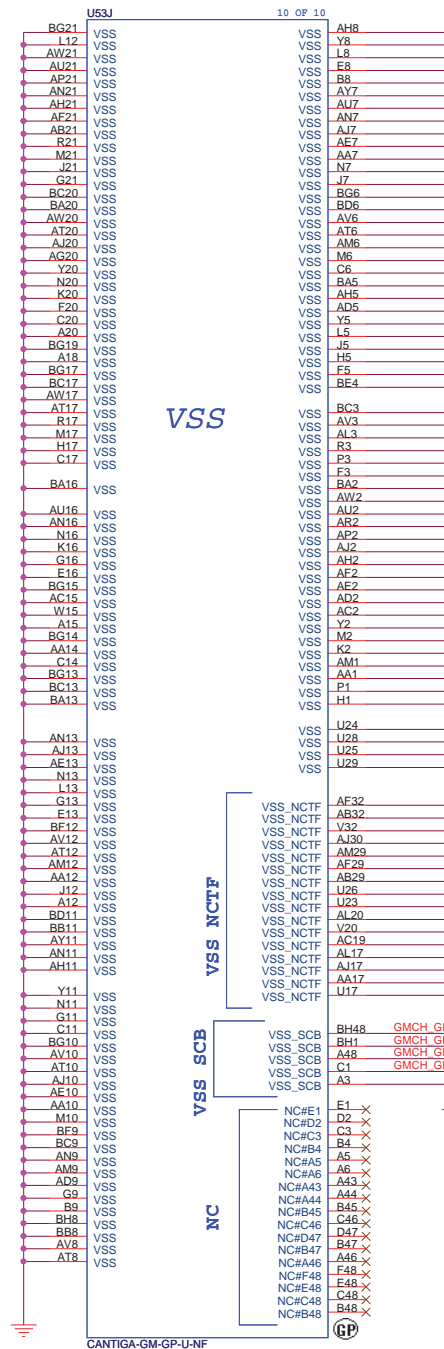
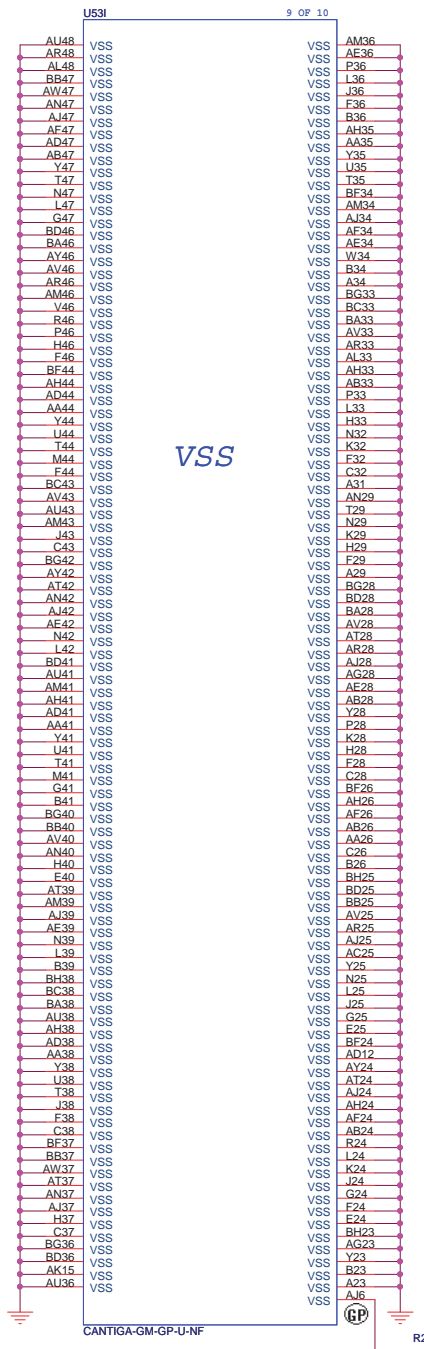


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Title			
CPU (3 of 3)			
Size	Document Number	Rev	
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Place them near to the chip (< 0.5")



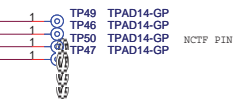


VSS

VSS NCTF

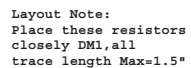
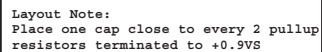
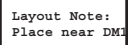
VSS SCB

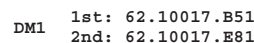
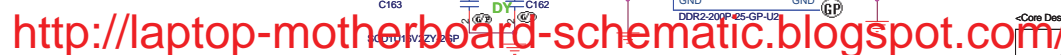
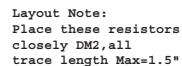
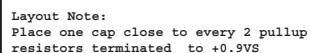
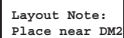
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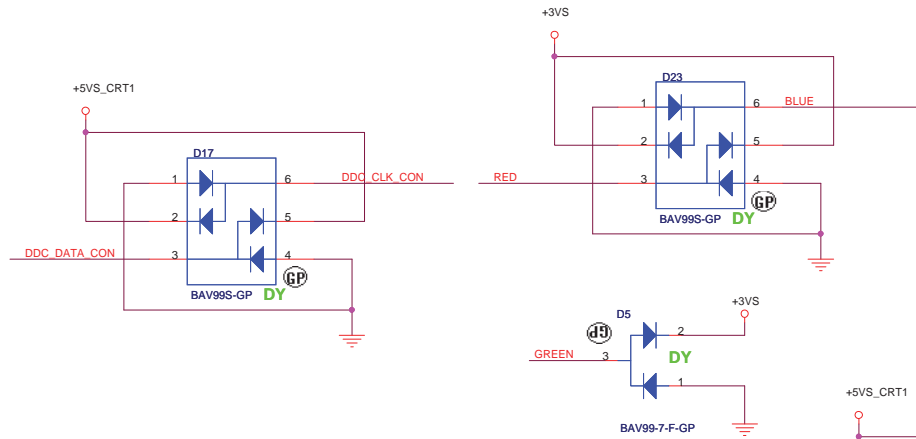




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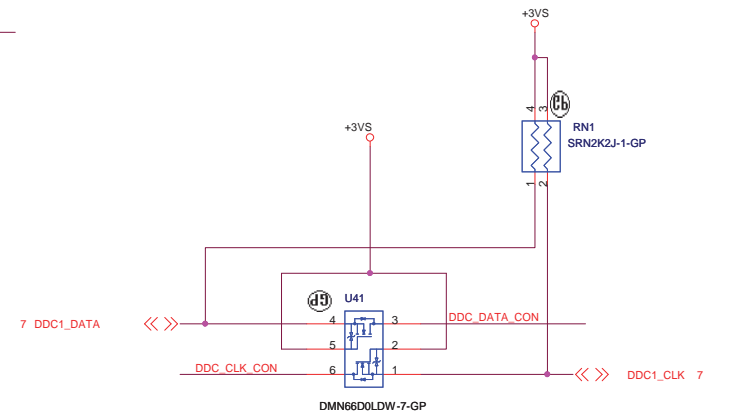
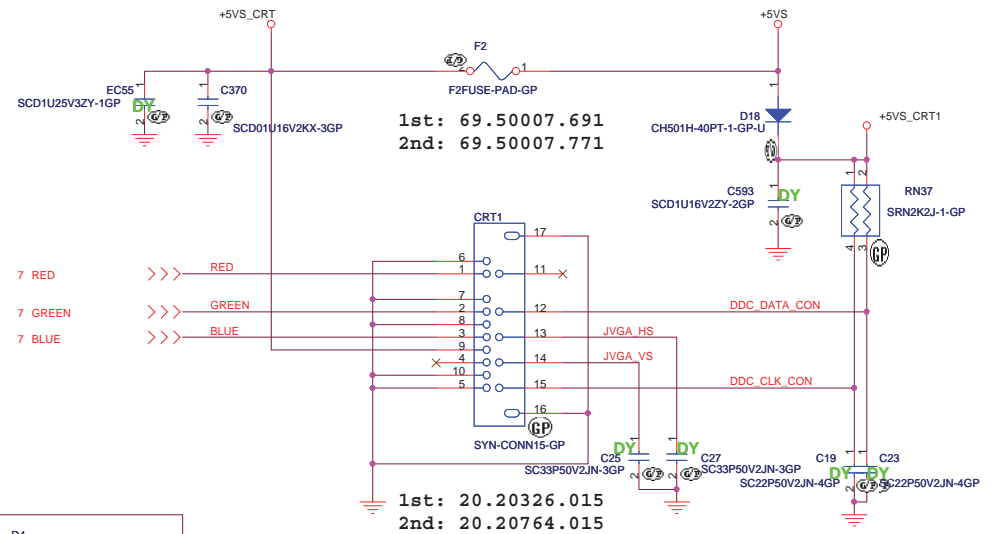
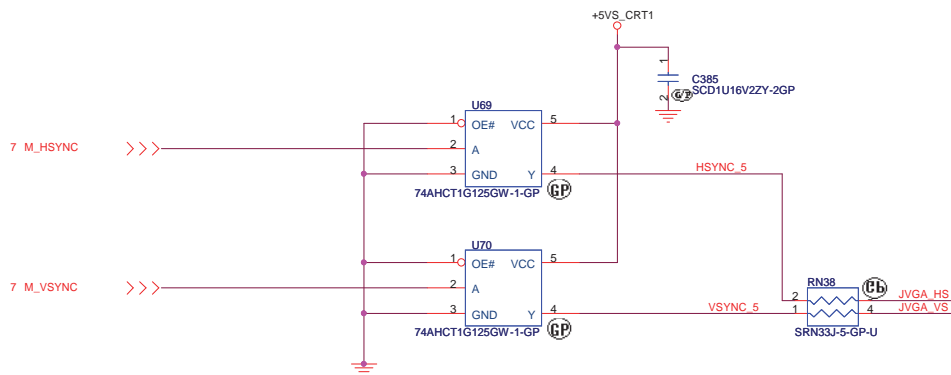
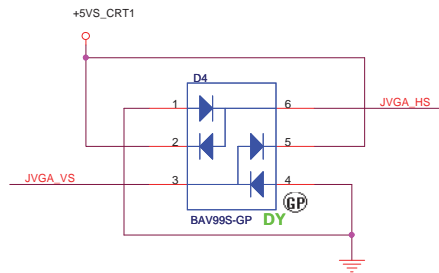
CRT I/F & CONNECTOR



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



5V @ ext. CRT side

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Title

CRT Connector

Size

Document Number

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Rev

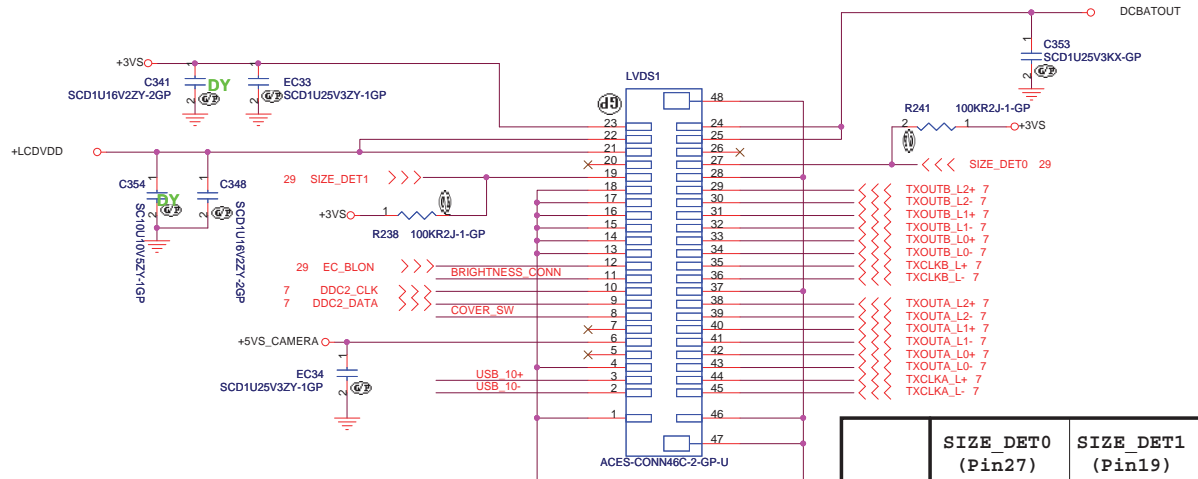
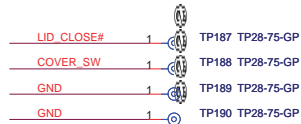
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Date: Thursday, July 09, 2009

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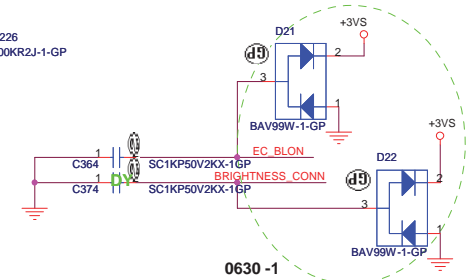
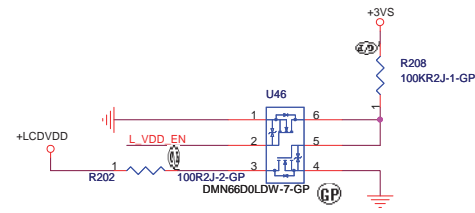
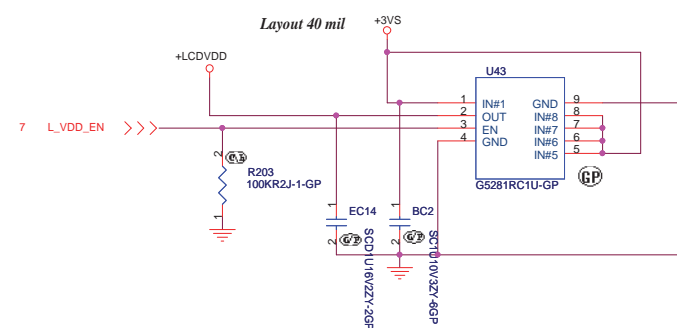
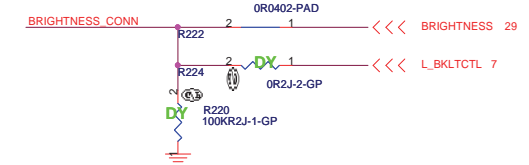
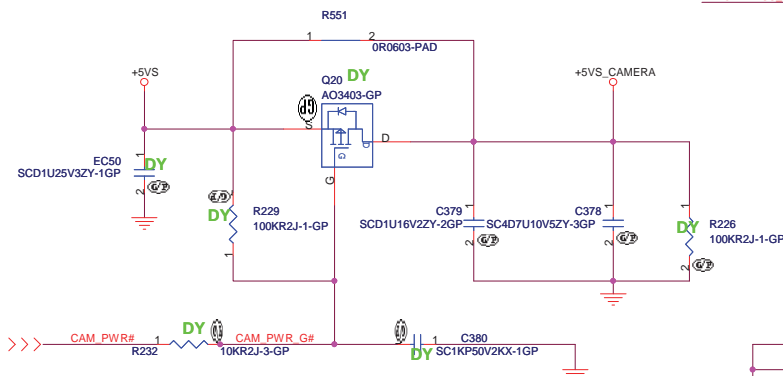
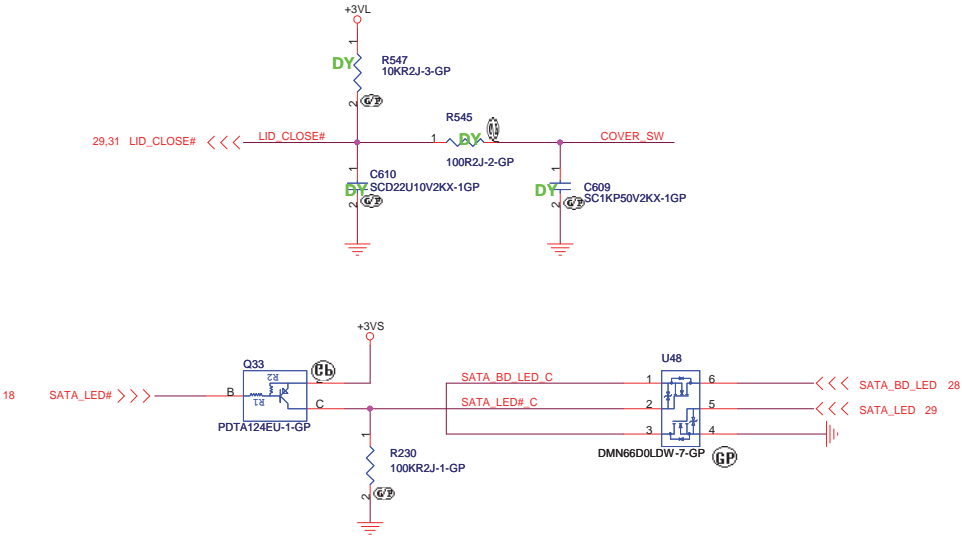
LCD / INVERTER INTERFACE / CAMERA

White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70



	SIZE_DET0 (Pin27)	SIZE_DET1 (Pin19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0

1st: 20.F1296.046
 2nd: 20.F1270.046



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Title: **LCD/Inverter Connector/CAM/LED**

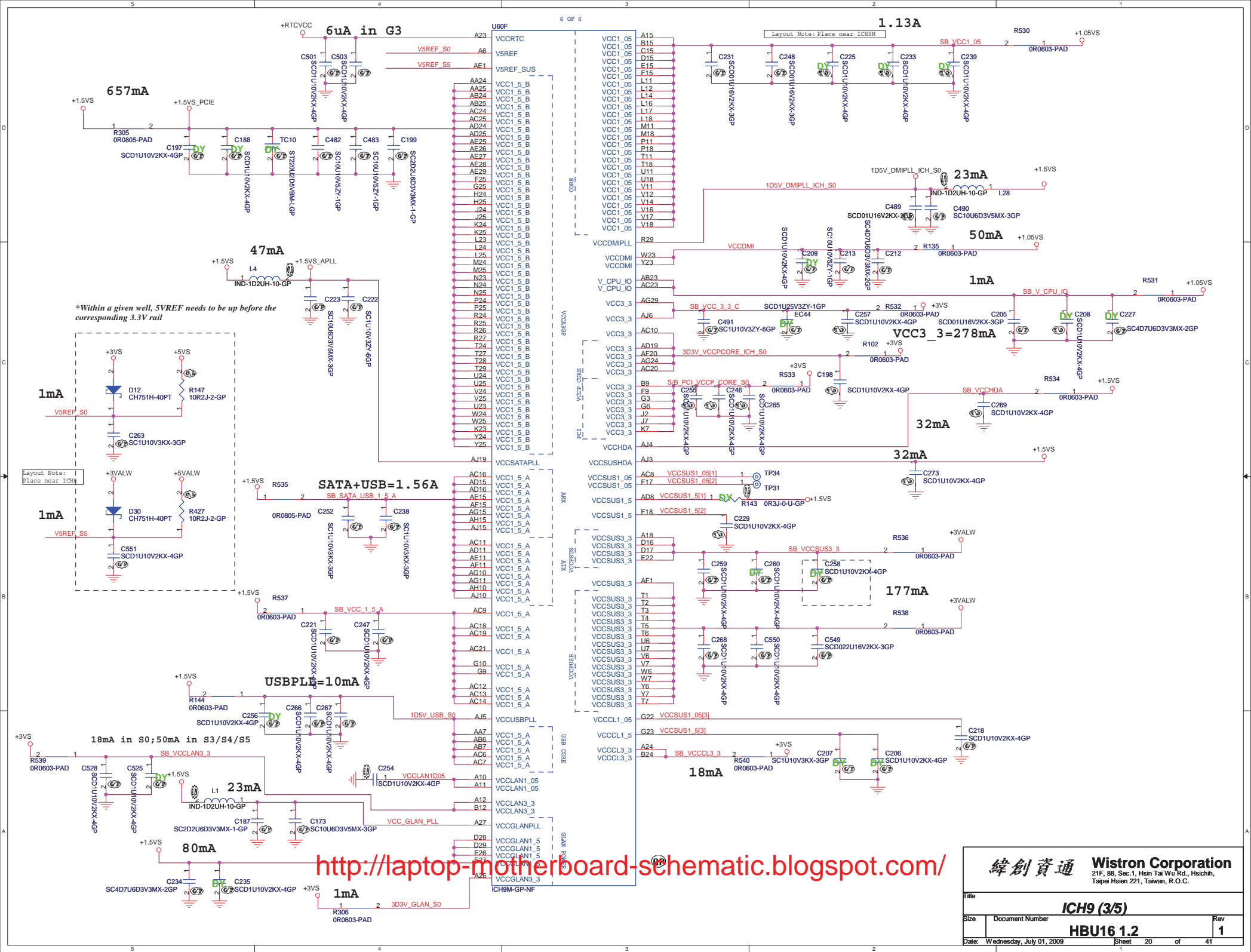
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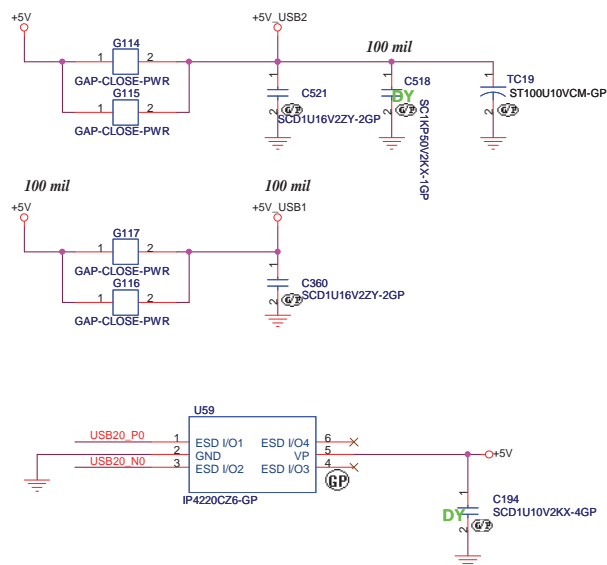




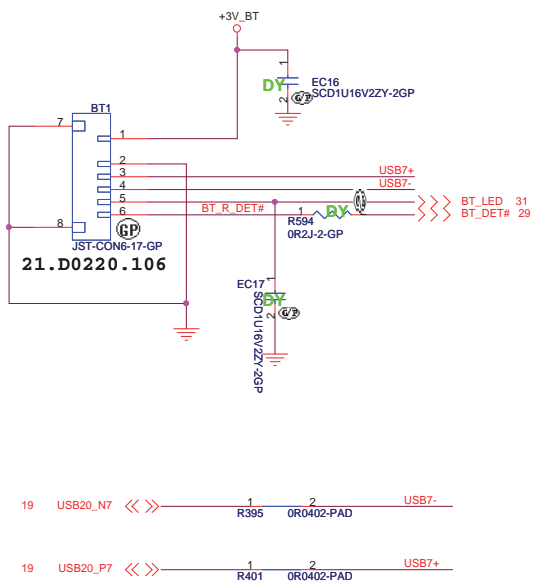


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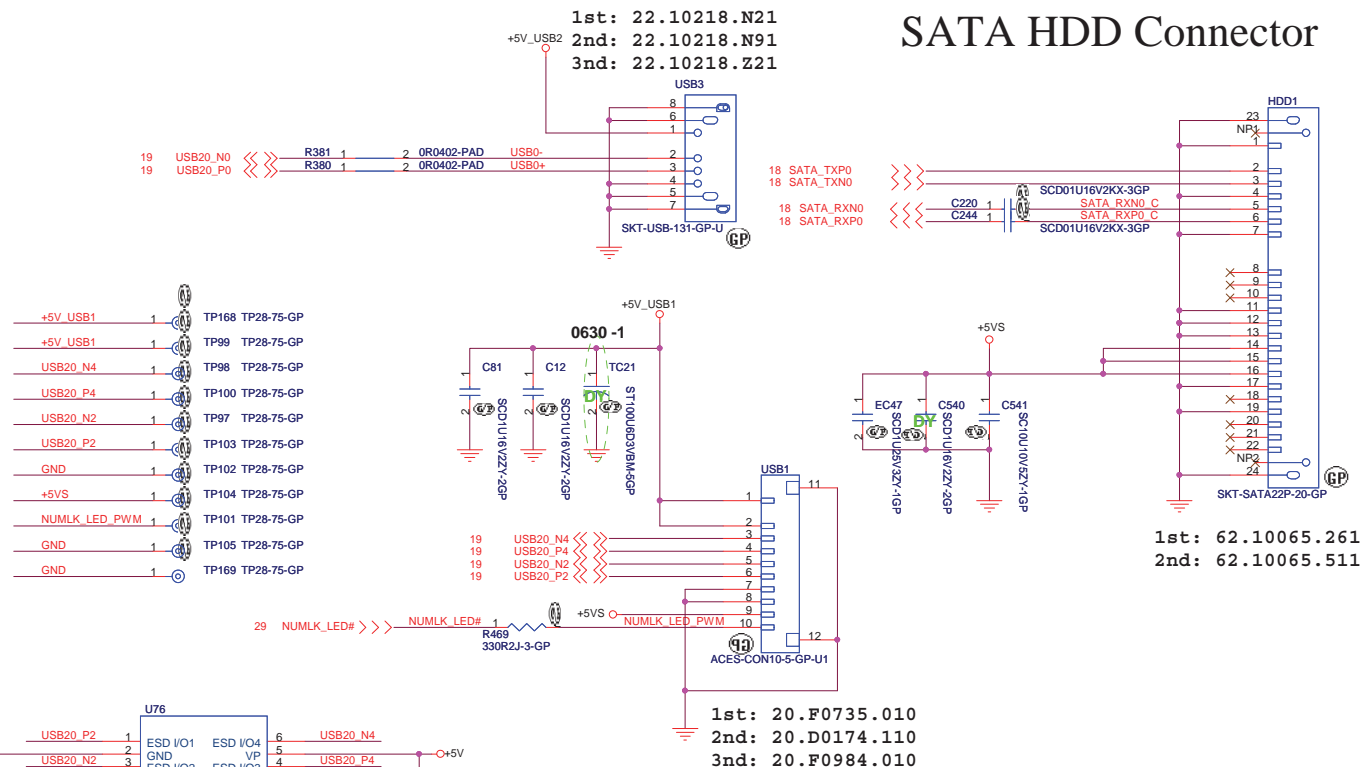
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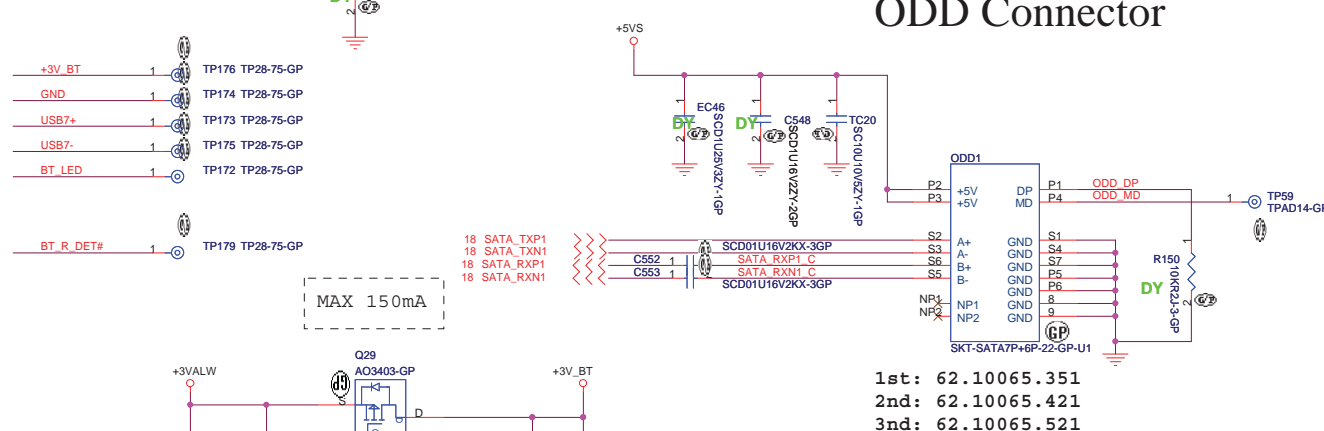
BLUETOOTH



SATA HDD Connector

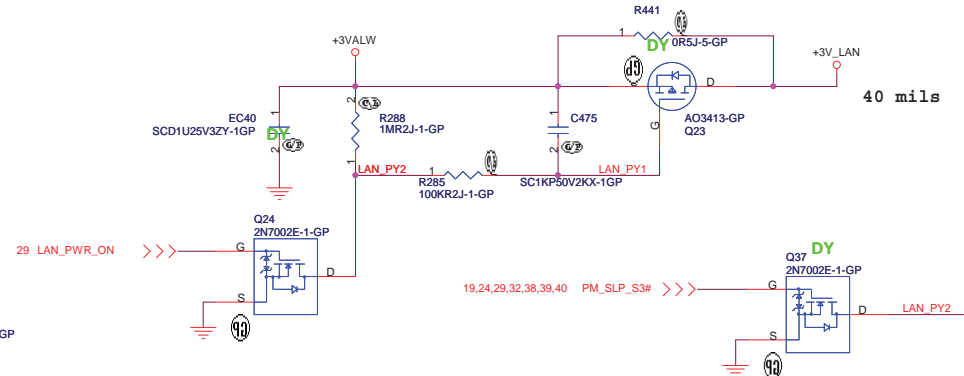
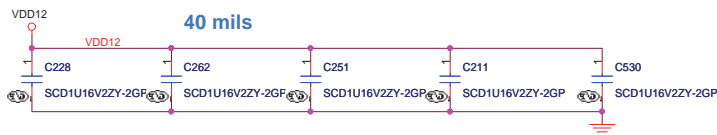
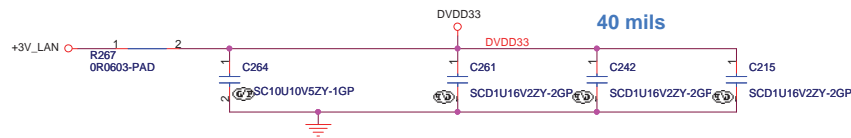


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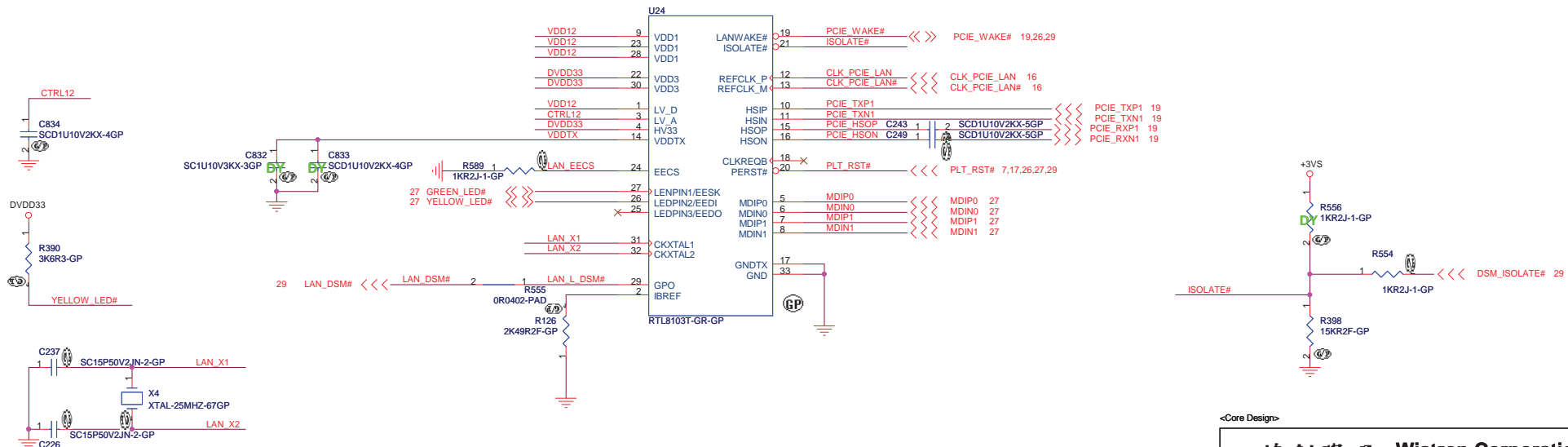


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HDD/CDROM/USB/BT	
Title Size A3 Date: Thursday, July 09, 2009	Document Number HBU16 1.2 Sheet 22 of 41
Rev 1	



EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED1 : LINK (Green)
=> LED2 : ACT (Yellow)
(BOTH 10/100 AND GIGA CHIP)



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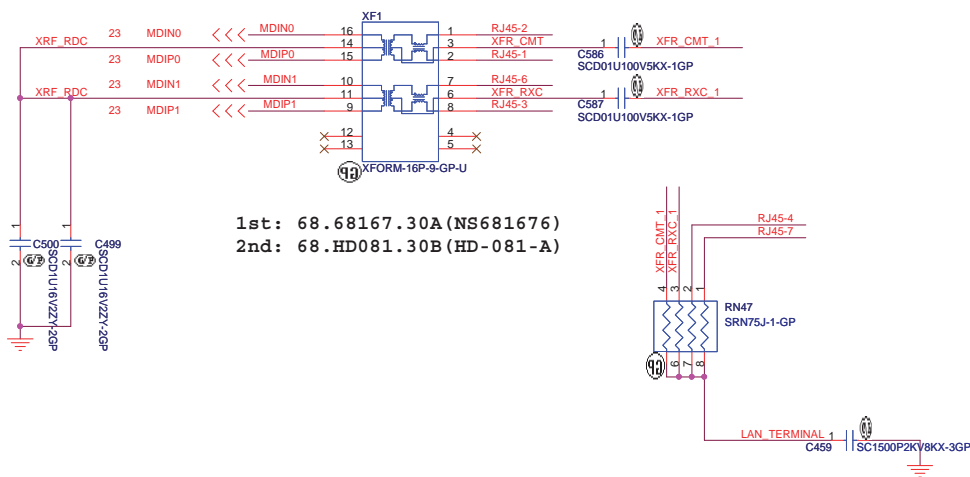
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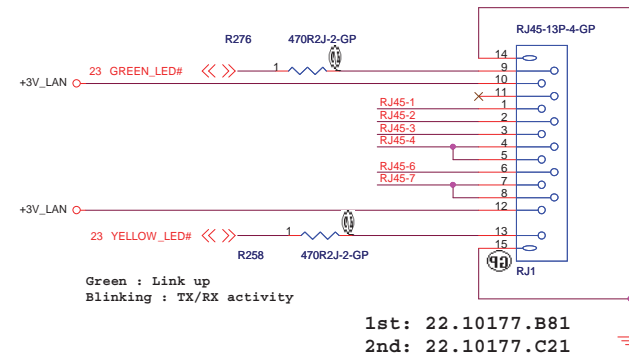
LAN Connector

10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal length.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

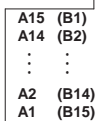
PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:

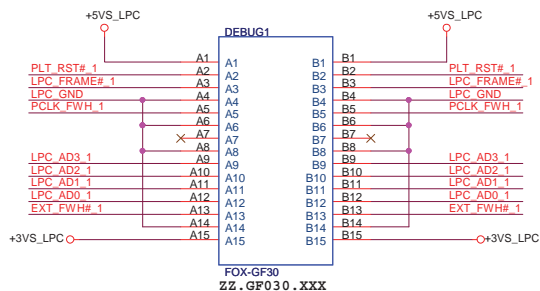
```
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.
```

Golden Finger for Debug Board

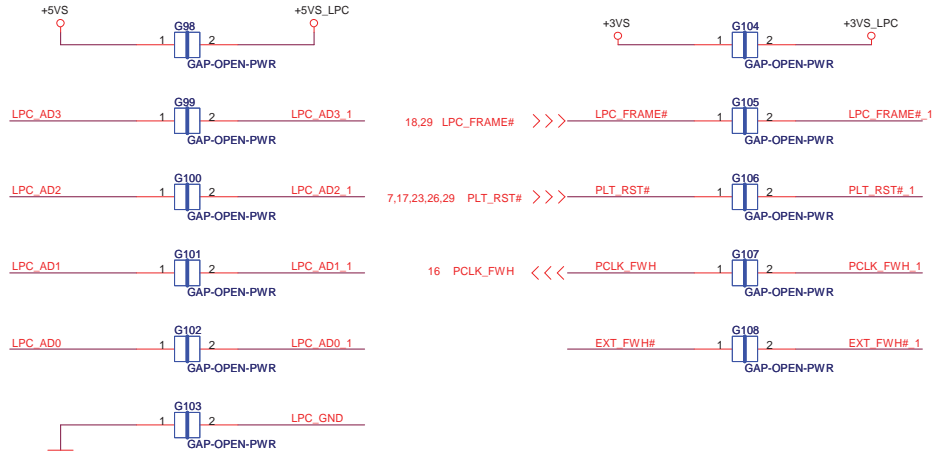
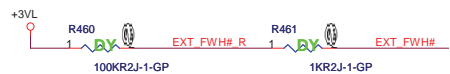


BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46



Please put near board edge.



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Title

LAN CONN/Debug

Size
A2

Document Number

HBU16 1.2

Rev

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Page: 113 of 113, 08/08/2008

100	20	5
E		

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PC BEEP GAIN CONTROL

GAIN	R568
-46 dB	DY
-18 dB	Install

SPDIF/BEEPAIN is an input used to set the PC BEEP gain while the device is in reset.

Default gain is -46 dB without populating the 10-Kohm pull-up resistor.

Note:
In order for the audio codec to Wake on Jack, the CODEC VAUX pin (VAUX_3.3, pin286) must be powered by a rail that is not removed unless AC power is removed.

7,18 HDA_RST#_CODEC >>>

7,18 HDA_BITCLK_CODEC
7,18 HDA_SYNC_CODEC
18 HDA_S0IN0
7,18 HDA_S0OUT_CODEC

Close to Modem

DY-MODM
R582 100K2J-1-GP
AUD_AGN

AUD_GPIO2
AUD_GPIO1
R165 10KR2J-3-GP
R161 10KR2J-3-GP
AUD_AGN

29 KBC_BEEP >>>
19 SB_SPKR >>>
1st: 83.R2003.E81
2nd: 83.BAT54.081
3nd: 83.00054.Q81

Close to SPKR1.

SPKR L+ C
SPKR L- C
SPKR R+ C
SPKR R- C
SRC100P50V-2-GP

SPKR L+ C
SPKR L- C
SPKR R+ C
SPKR R- C
TP91 TP28-75-GP
TP92 TP28-75-GP
TP93 TP28-75-GP
TP94 TP28-75-GP

Speaker

SPKR R- C
SPKR R+ C
SPKR L- C
SPKR L+ C
1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.D0209.104

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AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5VS_AUD to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

CLASSD_5V 2.5A (100mils)

CLASSDREF

0703-1

Close to U32.

Close to U32.

MIC

15,29 CAPS_LED# >>>

1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.F0689.004

1st: 20.K0320.015
2nd: 20.K0343.015

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AUDIO CODEC CX20583-11Z

Size Custom Document Number HBU16 1.2 Rev 1

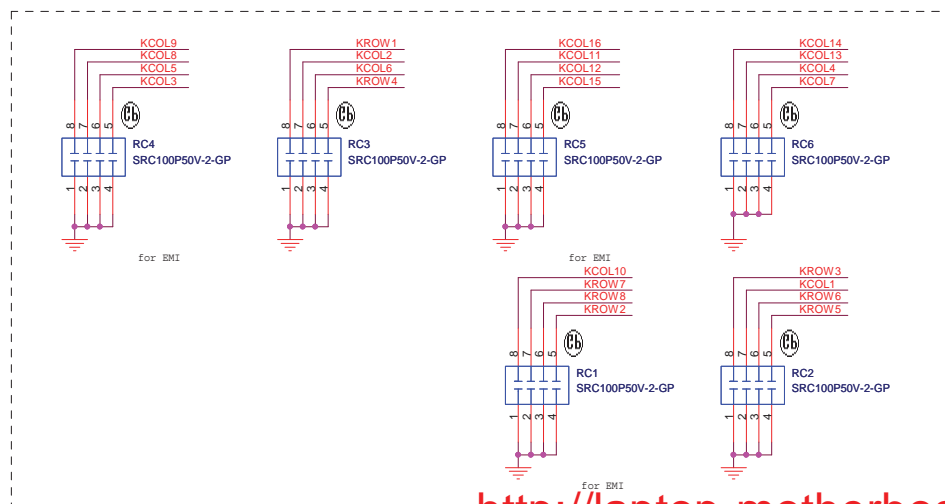
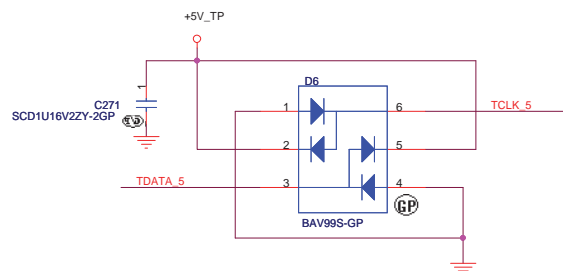
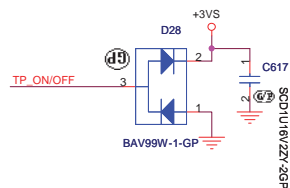
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Internal KeyBoard Connector

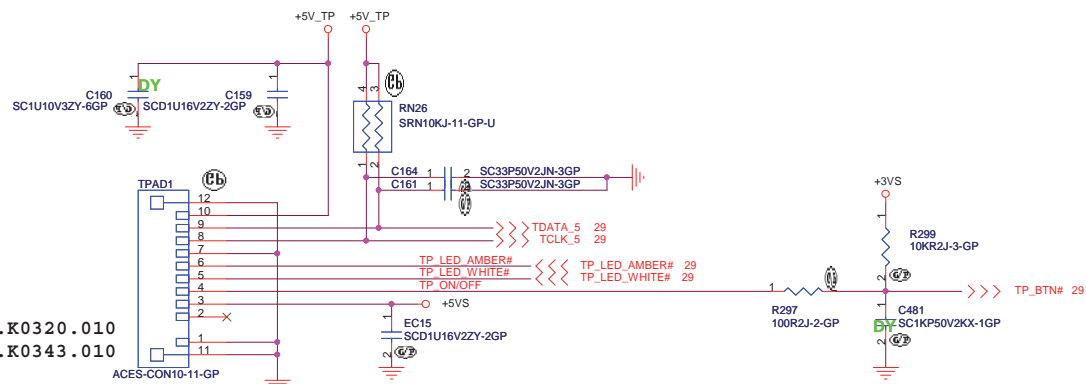
29 KROW[1..8] <<<=====
29 KCOL[1..18] <<<=====
29 KROW[1..8] <<<=====
29 KCOL[1..18] <<<=====

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



TouchPad Connector



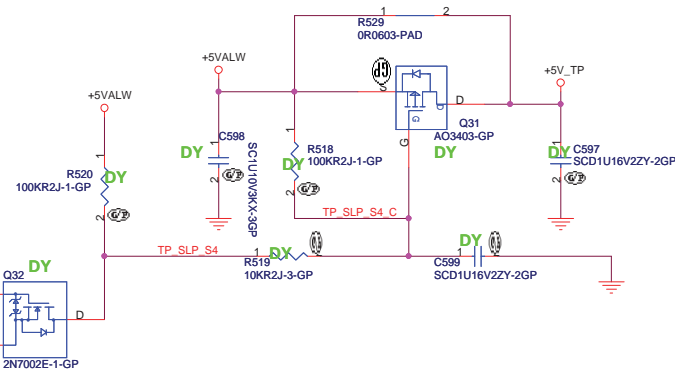
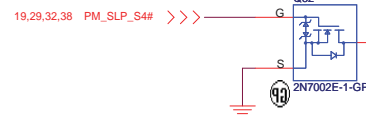
1st: 20.K0320.010
2nd: 20.K0343.010

1st: 20.K0345.026
2nd: 20.K0201.026

GND 1 TP185 TP28-75-GP
GND 1 TP186 TP28-75-GP

+5V_TP 1 TP83 TP28-75-GP
TDATA_5 1 TP84 TP28-75-GP
TCLK_5 1 TP85 TP28-75-GP
GND 1 TP106 TP28-75-GP
TP_LED_AMBER# 1 TP86 TP28-75-GP
TP_LED_WHITE# 1 TP87 TP28-75-GP
GND 1 TP107 TP28-75-GP
TP_ON/OFF 1 TP88 TP28-75-GP
+5VS 1 TP89 TP28-75-GP
GND 1 TP90 TP28-75-GP

Please populate close TPAD1



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Title

KeyBoard-CONN

Size

Document Number

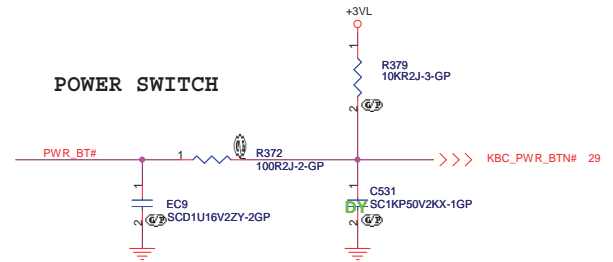
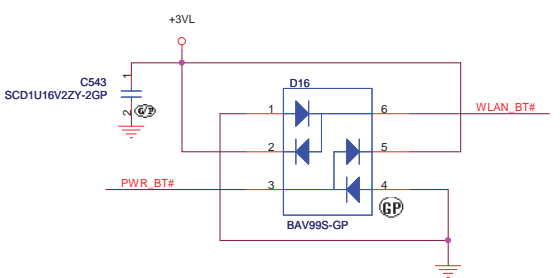
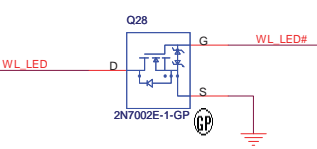
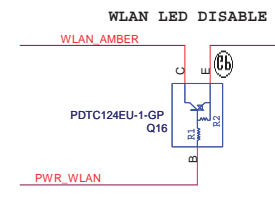
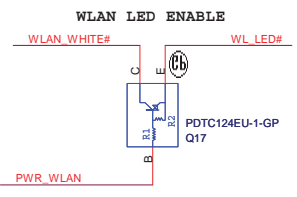
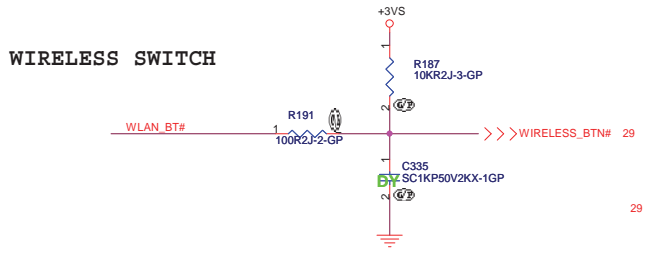
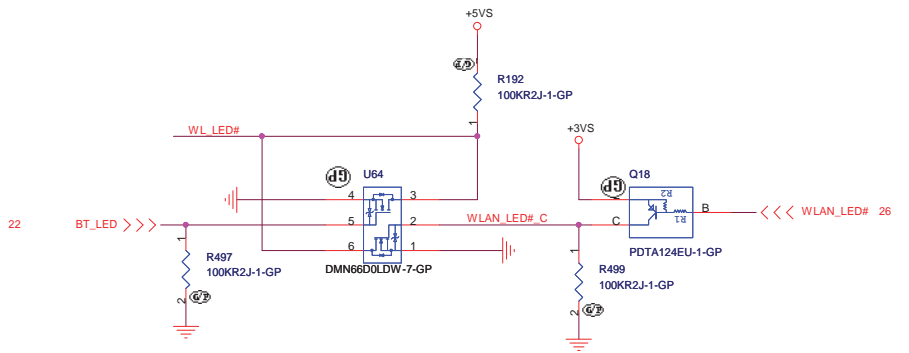
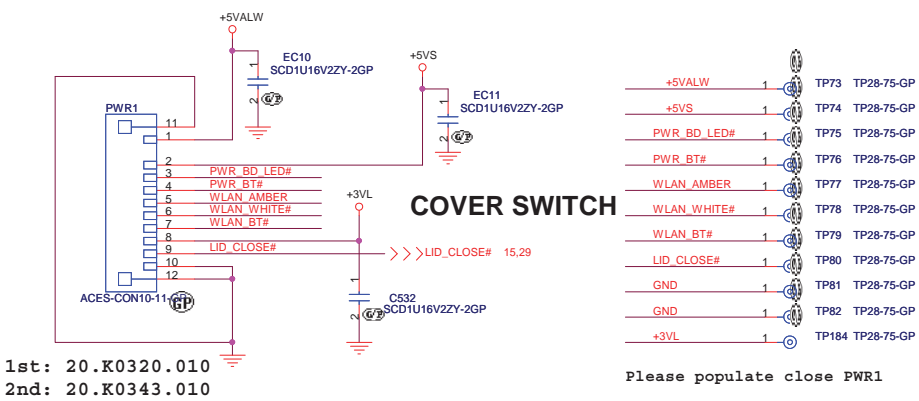
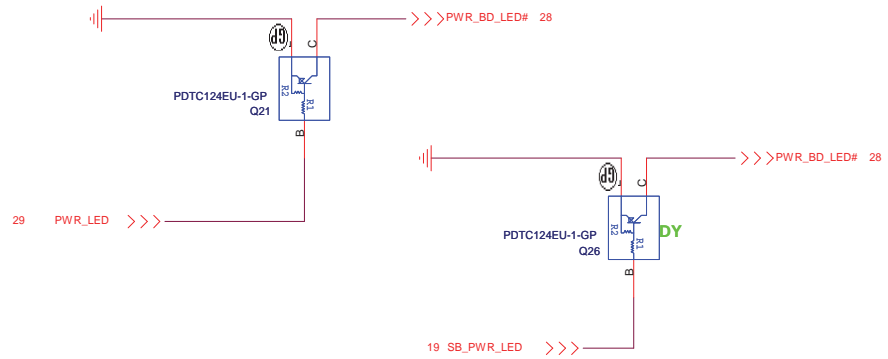
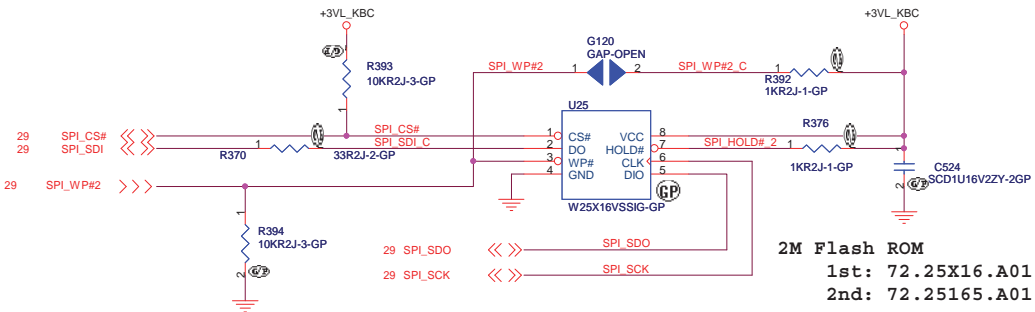
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Rev

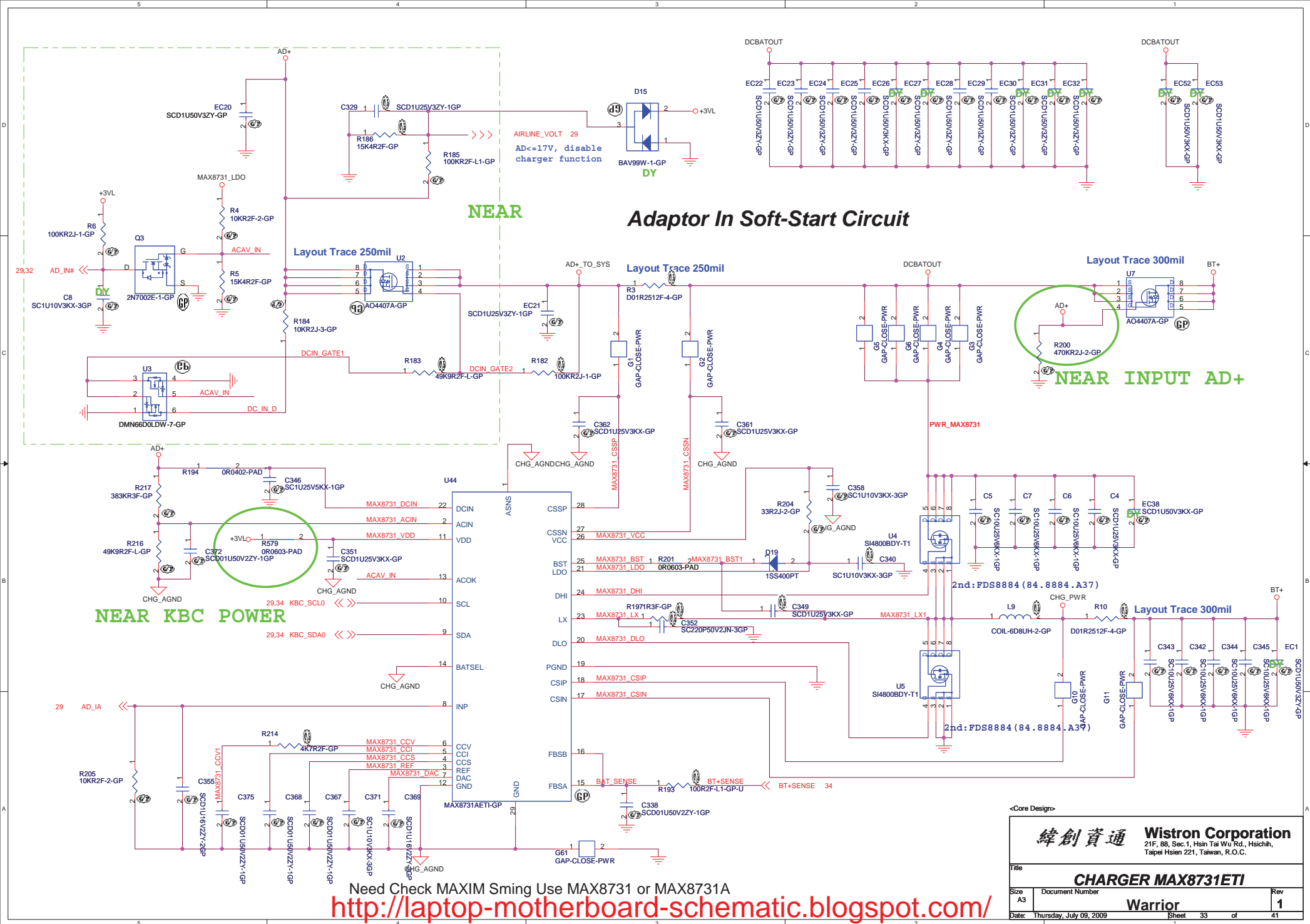
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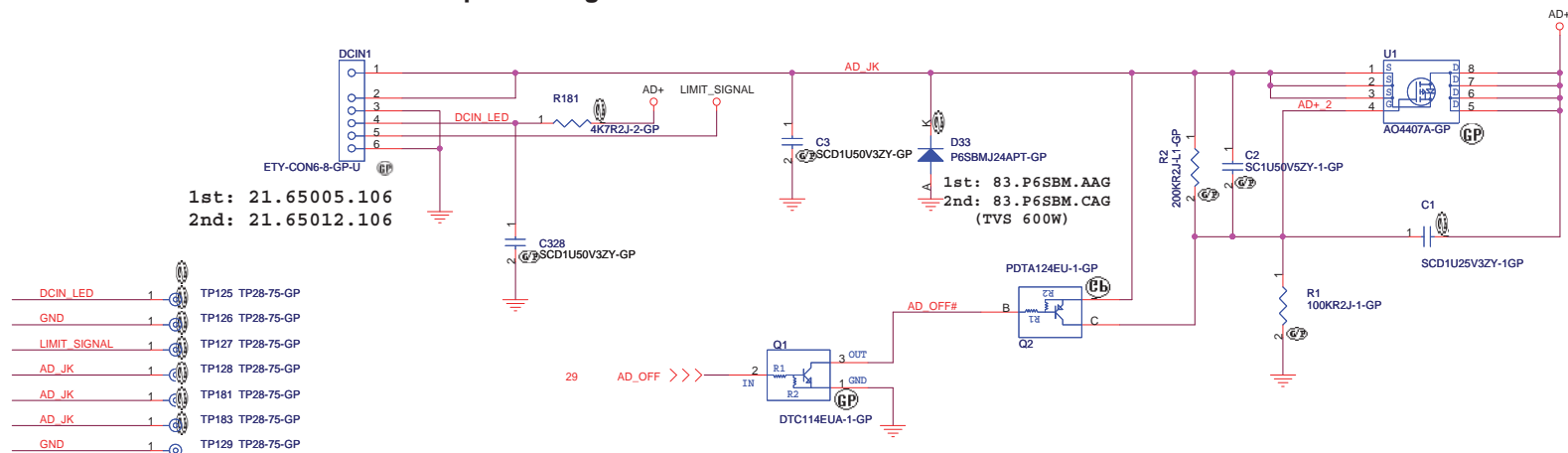


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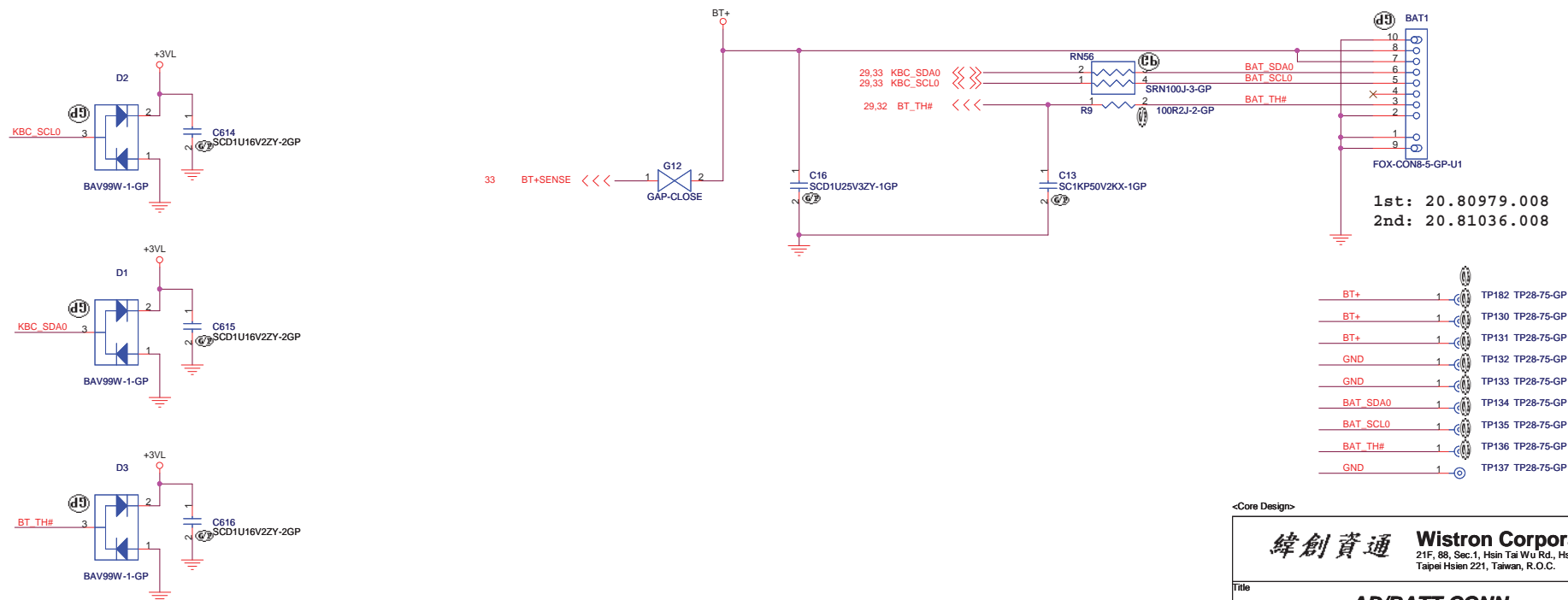


Need Check MAXIM Sming Use MAX8731 or MAX8731A
<http://laptop-motherboard-schematic.blogspot.com/>

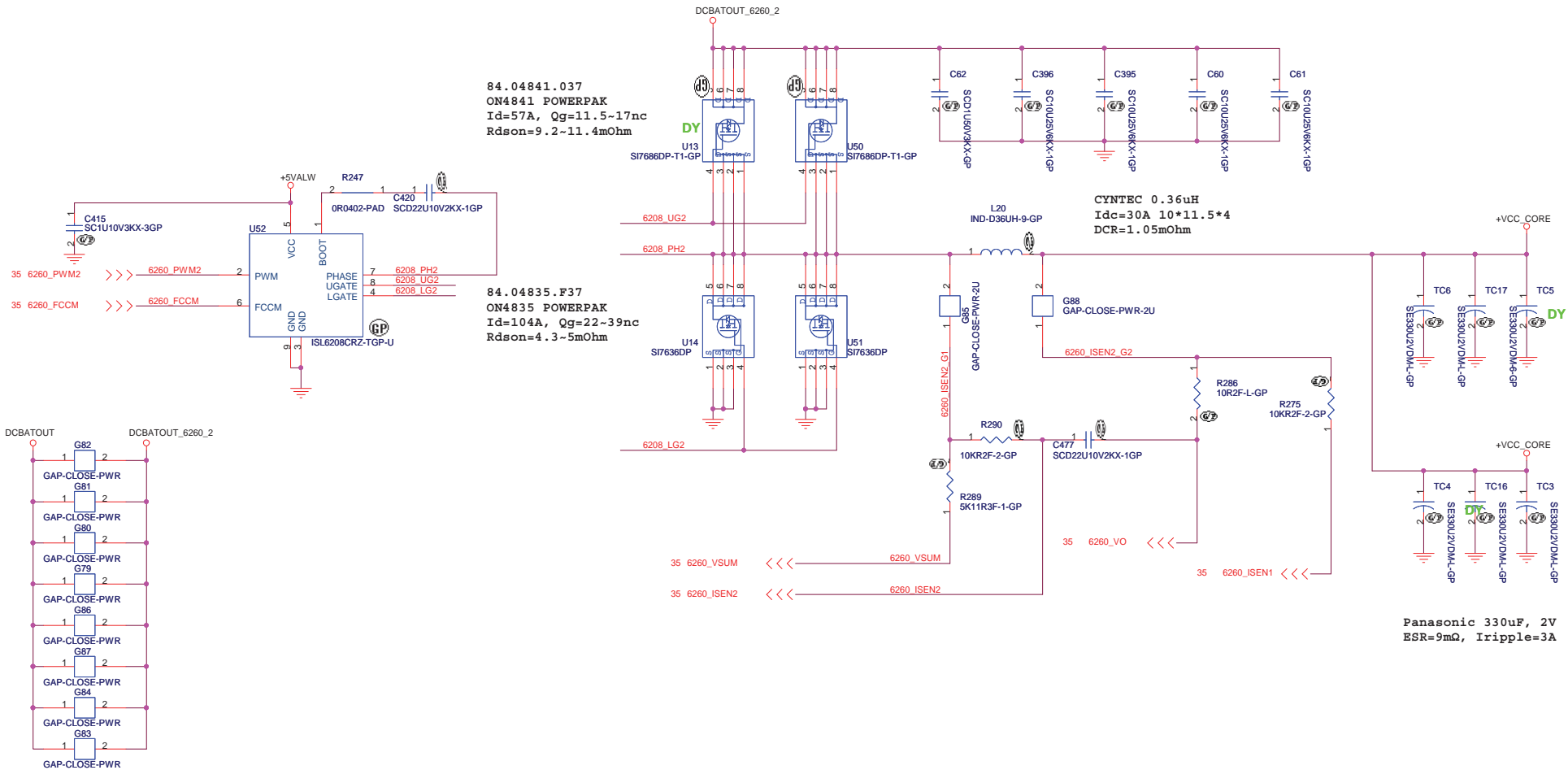
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BATTERY CONNECTOR



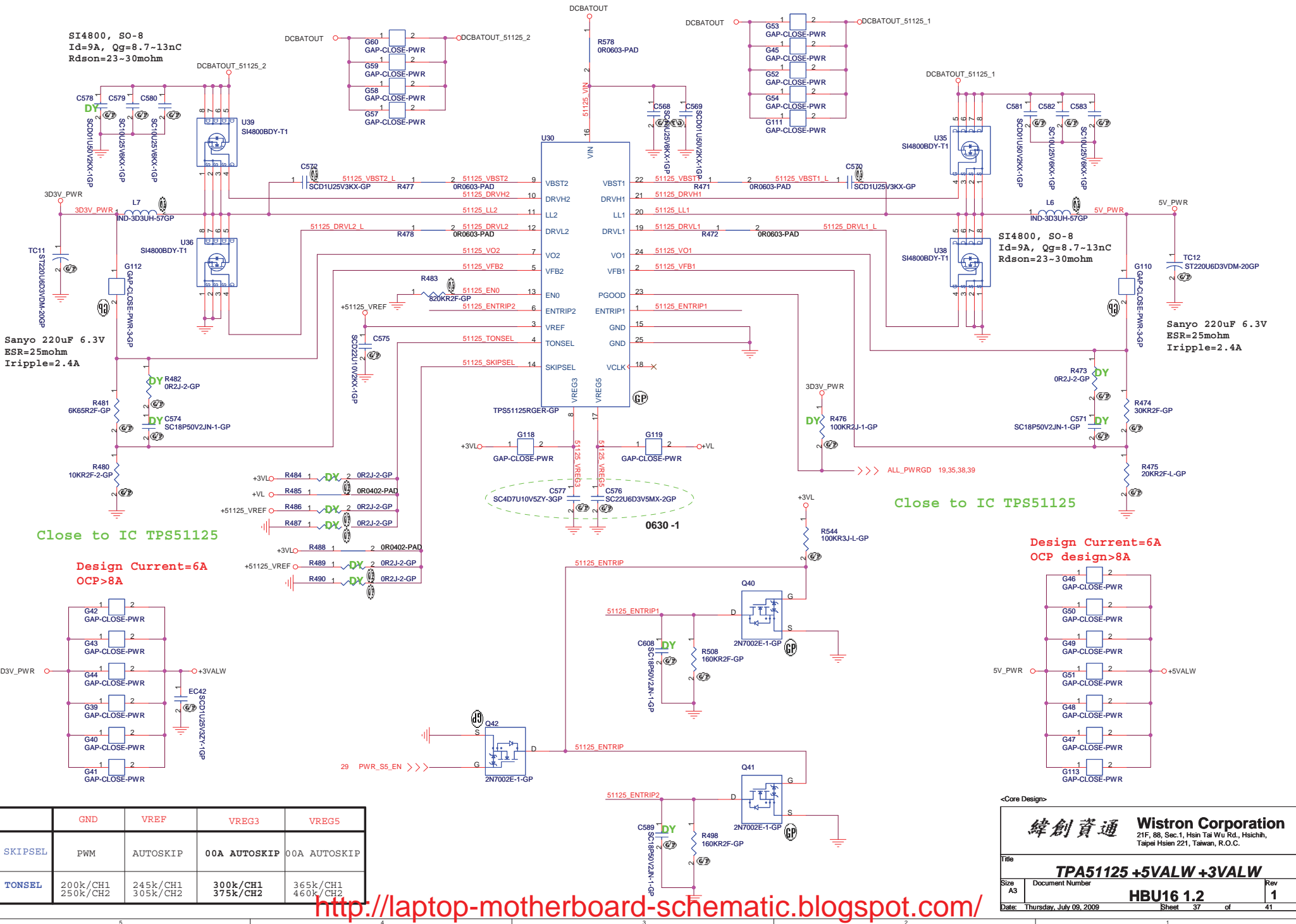
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Title			
ISL6260CCRZ CPU CORE(2/2)			
Size	Document Number	Rev	
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SI4800, SO-8
Id=9A, Qg=8.7-13nC
Rdson=23-30mohm



Close to IC TPS51125

Design Current=6A
OCP>8A

Close to IC TPS51125

Design Current=6A
OCP design>8A

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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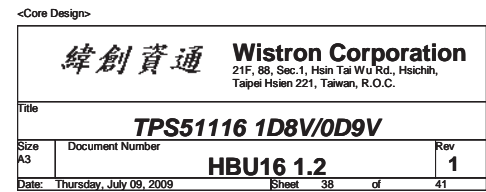
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

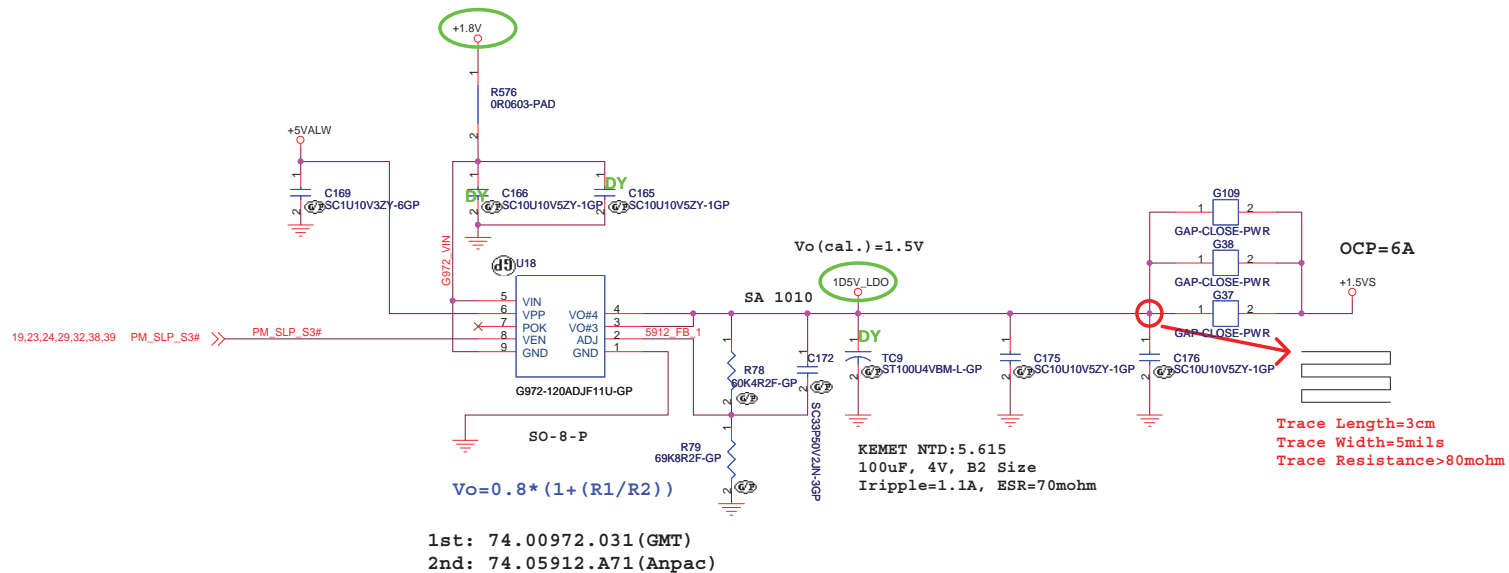
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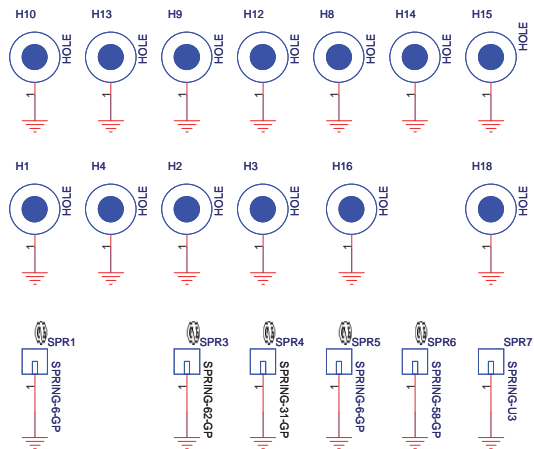
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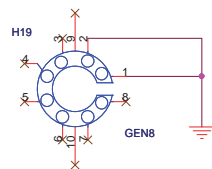


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Size	Document Number		Rev
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SPR1: 34.13B01.001,
 SPR3: 34.39S07.003, 34.39S07.101
 SPR4: 34.49U24.001,
 SPR5: 34.13B01.001,
 SPR6: 34.4B312.002, 34.4B312.101
 SPR7: 34.40U07.001, 34.40U07.101



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 Taipei Hsien 221, Taiwan, R.O.C.

Title				
MISC				
Size A3	Document Number			Rev
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